Astro Reconfiguration ISC

Version 1.0 January 2010

Capital Microelectronics, Inc.

Content

About This Guide

The Astro can support multi images in system configuration (ISC).It mean that the Astro can reconfigure the Astro using another Astro bitstream according to some conditions when Astro is running. The max image number is 8. The Astro has customized 8051 and fp_spi interface. User can implement the ISC function easily by using the 8051 to control the fp_spi interface which will operate the spi flash in Astro configuration process.

User can partition his design to some different but same function designs whose IO constraint is same. These different design bitstreams can be stored in spi flash. User can make use of the ISC feature to save fp resources. It is said that 1K logic cells can implement 8K logic cells logic using the Astro.

User'fp logic can operate the spi flash in user mode because the fp_spi has released the controlling of the spi flash. The customized 8051 has the standard spi interface which can operate 8 spi interfaces. So it is very easy for 8051 to erase, program, read the spi flash.

Astro Reconfiguration ISC

1. Introduction

The Astro can support multi images in system configuration (ISC).It mean that the Astro can reconfigure the Astro using another Astro bitstream according to some conditions when Astro is running. The max image number is 8. The Astro has customized 8051 and fp_spi interface. User can implement the ISC function easily by using the 8051 to control the fp_spi interface which will operate the spi flash in Astro configuration process.

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2. Block Diagram

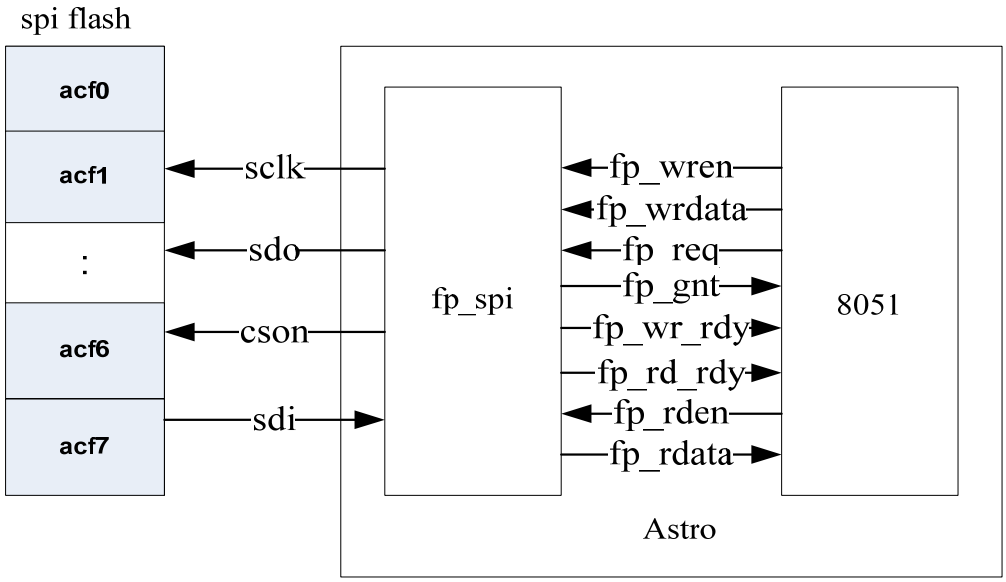

Fig 1 multi-image diagram

3. FP_SPI

User fp logic(8051 control the fp_spi interface)can write and read the fp_spi registers to control the ISC process.

Registers

Register Name	Address (10 bits)	R/W	Default value	Descriptions
TESTREG2	E	R/W	0x00000000	8051 code addres
TESTREG3	F	R/W	0x00000000	8051 code length
ISPCTRL	2f	R/W	0x00000000	[0]: ucr. [1]: uce. [7:2]: reserved. [10:8]: acfid. [31:11]: reserverd.
ACF0ADDR	30	R/W	0x00000000	acf0 address.
ACF1ADDR	31	R/W	0x00000000	acf1 address.
ACF2ADDR	32	R/W	0x00000000	acf2 address.
ACF3ADDR	33	R/W	0x00000000	acf3 address.
ACF4ADDR	34	R/W	0x00000000	acf4 address.
ACF5ADDR	35	R/W	0x00000000	acf5 address.
ACF6ADDR	36	R/W	0x00000000	acf6 address.
ACF7ADDR	37	R/W	0x00000000	acf7 address.

Table 1 Description of registers

FP_SPI Port

Port Name	Direction	Descriptions
fp_clk	i	clock, on posedge clock
fp_wren	i	write enable, high active
fp_wrdata	i	write data
fp_req	i	write request, high active
fp_gnt	o	bus grant,
fp_wr_rdy	o	write ready, high active
fp_rd_rdy	o	read ready, high active
fp_rden	i	read enable, high active
fp_rdata	o	read data

Table 2 Description of port

FP_SPI Waveform

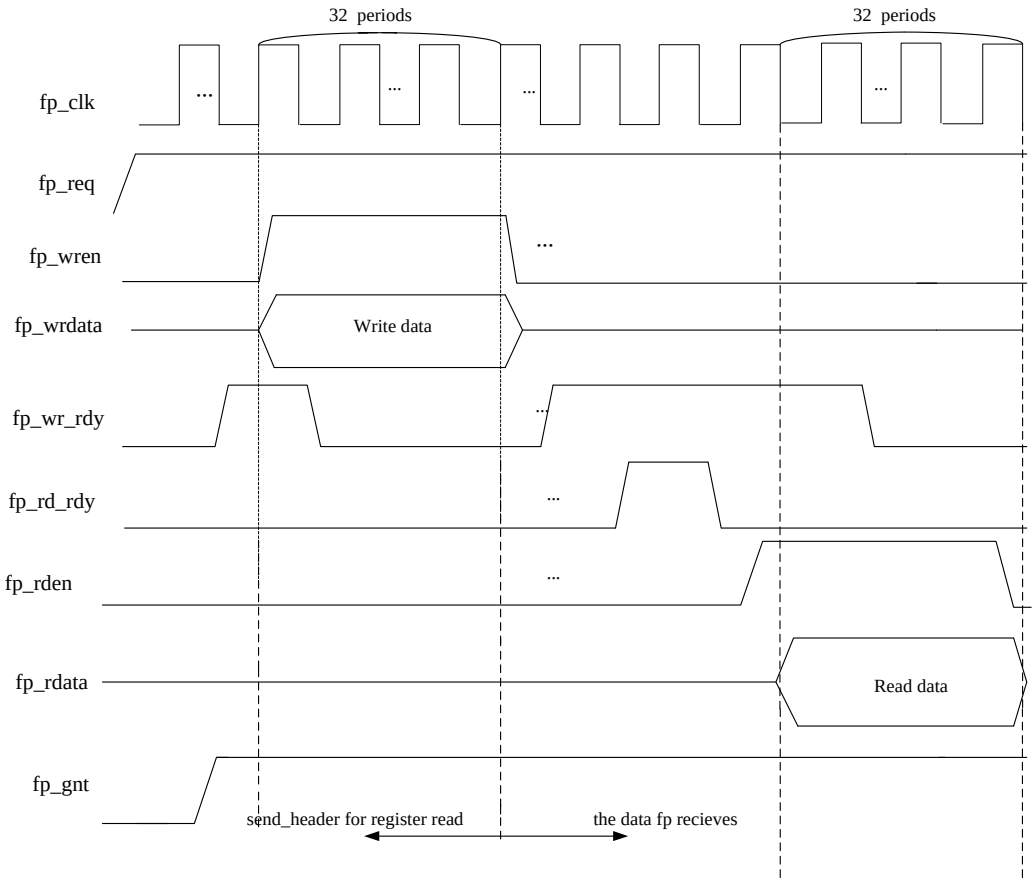

Fig 2 Waveform for FP_SPI read and write

Register Operation

There are write and read register operations.

The write 32 bit data is shifted in from lsb to msb. The read 32 bit data is shifted out from lsb to msb.

1. Write Register step:
   1) Write Header: The high 24 bit is the write command and the low 8 bit is the register NO. Refer to the Fig 2 and ISC.c.
   2) Write data, the data is also 32 bit.

2. Read Register step:
   1) Write Header: The high 24 bit is the read command and the low 8 bit is the register NO. Refer to the Fig 2 and ISC.c.
   2) Read data, the data is also 32 bit.

4. SPI FLASH

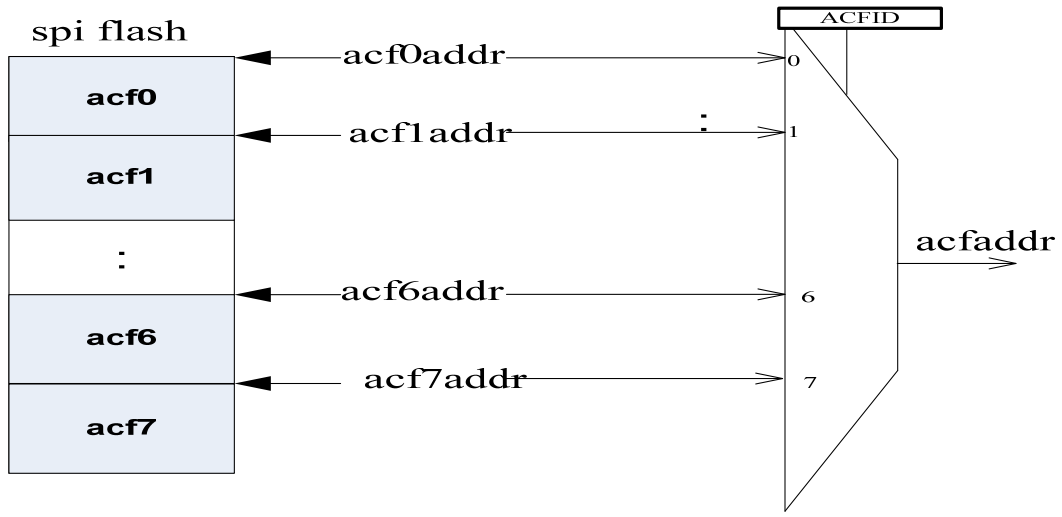

Fig 3 spi flash address map to register

User generates the several spi acf bitstream files and 8051 hex file. Then user can use Primace GUI to add and download all the acf files and the 8051 hex file to spi flash. The acf files are stored by sector, it is said that one acf will need integral sector, the values of the ACF0ADDR to ACF7ADDR are all the sector start address. The ACFID is ISPCTRL [10:8].User only use the ACFID to select the one of the acf which will configure the Astro.

Note: The download tool will generate a report which will tell user the actual address of the acf stored in the spi flash.

User can update the bitstream file in the spi flash from the address by 8051 erasing the sector and programming the spi flash. Then the system will work on the updated FP function when power on.

5. 8051

The Astro has 1K logic cells, 2 1Kx8 EMB and 8051. The 8051 is use as the ISC controller to control the fp_spi interface and spi master to access the spi flash and write the 8051 code to SRAM.

The 8051 will generate the waveform to control the fp_spi to reconfigure the Astro from one of the bitstreams which are stored in the spi flash when the 8051 get reconfiguration command. The 8051 C calls are in the ISC.h and ISC,c. User can add the ISC.c to his project and call the ISCReq () call. The fp_spi signals are control by Port bit.

The ISC function only use the ISPCTRL 2f register. Call the ISCReq ( )to write the register a

correct data, then the fp_spi can reconfigure the Astro from your selected image.

Example1:

ISCReq (1); // Select the second Astro bitstream from the spi flash to reconfigure the Astro.

Example2:

ISCReq (7); // Select the NO.8 Astro bitstream from the spi flash to reconfigure the Astro

```
void  ISCReq (INT8U id)  // id is write to the ACFID
{
    INT32U ddata;
#ifdef    OTP_ISC
#else

    ddata = id << 8;
    ddata = 0x00000003 | ddata;
    ISC_REQ = ISC_HIGH; // request enable
    ISCClk (12);
    ISCWriteBit32(0x22007c2f);
        ISCWriteBit32(ddata);
    ISC_REQ = ISC_LOW; // request disable
    ISCClk (12);
#endif
}
```

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Technical Support Assistance

Tel: +86 10 82150100

E-mail: support@capital-micro.com

Website: www.capital-micro.com