1. Introduction

CME-M7 devices have 3 configuration modes: JTAG, AS and PS mode. In the PS mode, CME-M7 family works as a slave device, receives configuration data from external master controller passively. SPI Master cannot read configuration data from CME-M7 family.

2. Configuration Mode and Pins

The bitstream is loaded into the device through special configuration pins. These configuration pins serve as the interface for a number of different configuration modes:

There are 3 configuration modes: JTAG, AS and PS mode. AS, PS mode configuration are controlled by a mode-select pin CFG_MODE, as described in table below.

Note: CME-M7 family with FLASH only provides 2 modes, AS and JTAG.

Table 1 Configuration Mode

Mode select pin CFG_MODE	Mode	Description
0	AS	Active Serial mode. The chip will be configured automatically. Configuration data is stored in the SPI flash.
1	PS	Chip acts as slave. External microcontroller feeds configuration data into the chip.
0/1	JTAG	JTAG-based configuration. This mode takes high privilege over AS and PS modes

Certain pins are dedicated to configuration (Table above), while others are multi-function pins (Table below).The multi-function pins serve both as configuration pins and as user I/O after configuration. The dedicated configuration pins retain their function after configuration.

Table 2 Configuration Pins

Multi-Function Pins: SPI serial configuration Pins		
FLS_SCLK	Input/output	In passive serial configuration mode, SCLK is a clock input used to clock configuration data from external device source into device. In active serial configuration mode, SCLK is a clock output from device. The pin can be used as regular user I/Os after configuration.
FLS_SI	output	Dedicated configuration data output pin in AS mode. No configuration function in PS mode. The pin can be used as regular user I/Os after configuration in AS mode
FLS_SO	Input	Serial data input from external master in PS mode or from spi flash

Multi-Function Pins: SPI serial configuration Pins		
		in AS mode. The pin can be used as regular user I/Os after configuration.
FLS_CSN	output or input	Chip select output to enable a SPI Flash in AS mode or input as a CME-M7 device select. This output is used during AS mode. The pin can be used as regular user I/Os after configuration in AS mode. it is used as chip selection control (input) during PS. The pin can be used as regular user I/Os after configuration in PS mode.
FLS_WP	Input/output	Write Protect Output (Data Input Output 2)
FLS_HOLD	Input/output	Hold Output (Data Input Output 3)
Dedicated Configuraiton Pins:		
CONF_DONE	output	This is a dedicated configuration status pin, the pin will output high during configuration. The pin can be used as regular user I/Os after configuration.
CFG_MODE	input	0: Active Serial mode, 1 Passive Serial mode. The pin can be used as regular user I/Os after configuration.
nCONFIG	input	Chip global reset input. Active low.
Dedicated Pins: JTAG		
TCK	input	TCK Input Boundary-Scan Clock.
TDI	input	TDI Input Boundary-Scan Data Input.
TDO	output	TDO Output Boundary-Scan Data Output.
TMS	input	TMS Input Boundary-Scan Mode Select.

3. PS Scheme

The PS schematic is shown below. The CME-M7's SPI configuration interface is a separate, independent I/O bank, powered by the VDD33 supply input. Typically, VDD33 is the same voltage as the application processor's I/O. The configuration control signals, CFGDONE and nCONFIG, are supplied by the separate I/O Bank 2 voltage input, VDDIO_2.

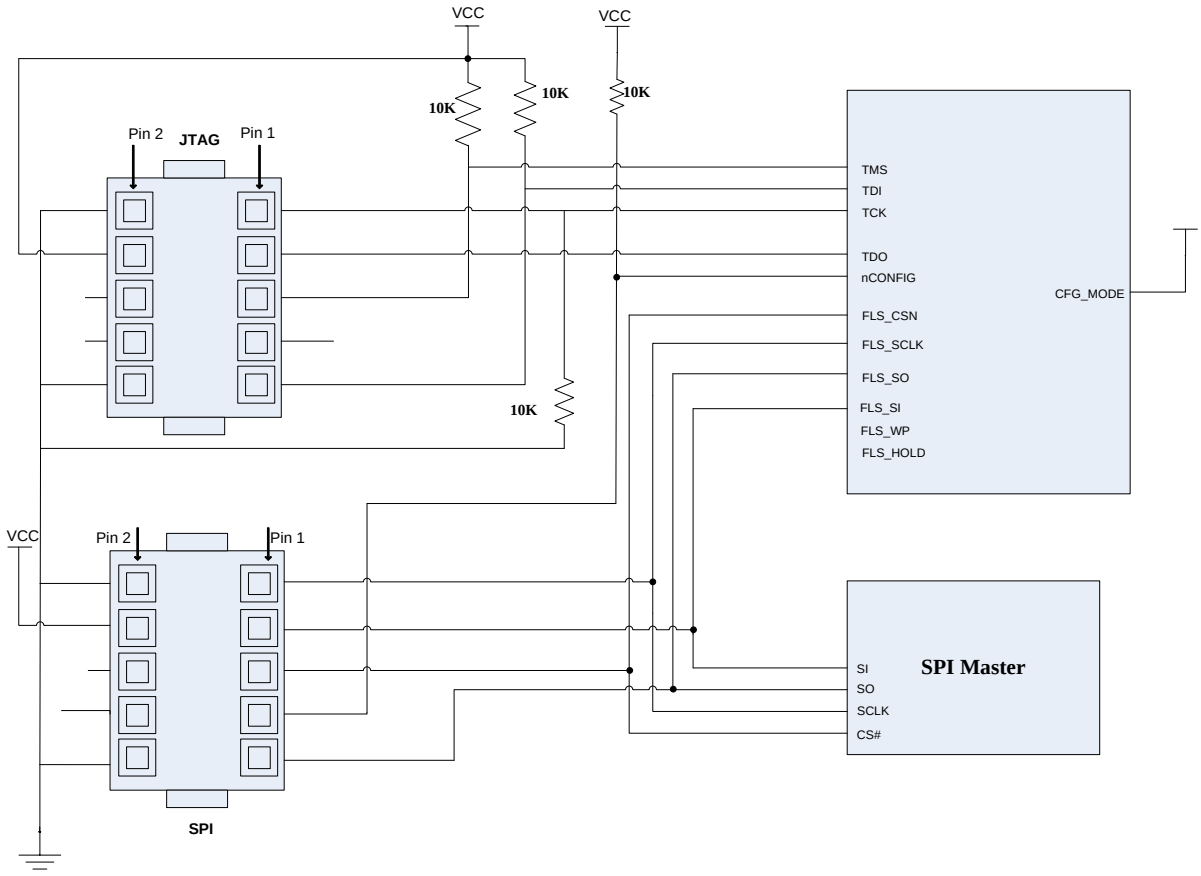

Figure 1 PS schematic

4. PS Configuration Process

You can perform PS configuration on CME-M7 device family with an external intelligent host, such as a microprocessor with flash memory. In the PS scheme, an external host controls the configuration process. After configuration, the SPI port pins are available to the user-application as additional GPIO pins, supplied by the VDD33 input voltage.

Figure 2 illustrates the interface timing for the PS mode.

1) Reset process. The application host begins by driving the CME-M7 nCONFIG pin low, resetting the CME-M7 FPGA. Similarly, the host holds the CME-M7's FLS_CSN pin Low. The host must hold the nCONFIG pin low for at least 500 ns. Ultimately, the host either releases the nCONFIG pin and allows it to float High via the 10 KOhm pull-up resistor to VCCIO_2 or drives nCONFIG High. The CME-M7 FPGA enters PS mode when the nCONFIG pin returns High while the CFG_MODE pin is Low.

2) Initialization process. After driving nCONFIG High or allowing it to float High, the host must wait a minimum of 1250 µs, allowing the CME-M7 device clears the internal configuration memory.

3) Clock switch process. After the initialization process, the host must drive the FLS_CSN to high and the high time is 8 FLS_SCLK cycles.

4) Configuring internal configuration memory process. After the configuration clock is switched to FLS_SCLK, the host sends the configuration image (*_ps.acf) generated by the Primace. The host must place the configuration data one bit at a time on the FLS_SO pin at the negedge of the FLS_SCLK. The most-significant bit (MSB) of each byte must be sent first. For example, if the configuration data *.acf contains the byte sequence 02 1B EE 01 FA, the serial bitstream you must send to the device is:

   0000-0010 0001-1011 1110-1110 0000-0001 1111-1010

   CME-M7 device family receives configuration data on the FLS_SDI pin and the clock is received on the FLS_SCLK pin. Data is latched into the device on the rising edge of SCLK. Data is continuously clocked into the target device until all the configuration data is sent and the FLS_CSN is driven to high.

5) Addition dummy process. After sending the entire image, the CME-M7 FPGA CONF_DONE goes high and the device enters the user mode. If the CONF_DONE pin remains Low, then an error occurred during configuration and the host should handle the error accordingly for the application. The host must send extra 64 FLS_SCLK clock cycles measured from rising-edge to rising-edge to CME-M7 device. After the additional FLS_SCLK cycles, the SPI interface pins then become available to the user application loaded in FPGA.

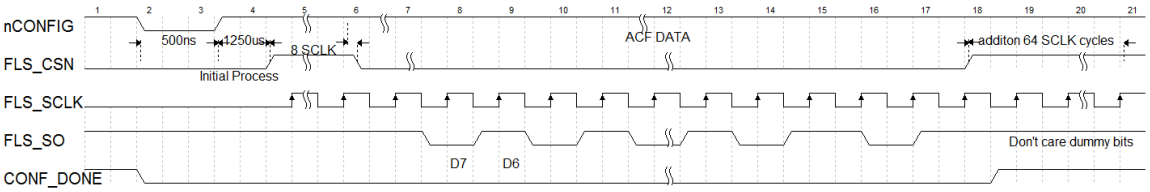

Figure 2 PS Configuration Waveform

To reconfigure the CME-M7 FPGA or to load a different configuration image, merely restart the configuration process by pulsing nCONFIG Low or power-cycling the FPGA.

The max PS FLS_SCLK clock frequency is about 25MHz.

5. PS Configuration Reference Code

The PS code example is shown below. The 8051 MCU PS host uses the GPIO to control the PS master's signals. The below code signals are from the master's point of view. The LBA_Buff array

#define CS P0_0 //CS

#define SDO P0_1 //SDO

```
#define SCLK P0_2 //SCLK
#define nCONFIG P0_3 // nCONFIG
#define FILE_LEN        0xAB000

unsigned char M7_PS_pre_clk;
unsigned int i;
unsigned char i_mask;
unsigned char bit_mask;

nCONFIG = 1;
CS=0;
SDO =1;
SCLK =1;
//Reset process
CS=0;
nCONFIG = 0;
Delay1us();
nCONFIG = 1;
//Initialization process
Delay1250us();

// Clock switch process
CS=1;
for(M7_PS_pre_clk=0;HR3_PS_pre_clk<8;HR3_PS_pre_clk++) //M7 8=pass
{
        SCLK=0;//clk
        Delay1us();
        SCLK=1;//clk
        Delay1us();
 }
 CS=0;    //cs
// Configuring internal configuration memory process
```

```
for(i=0;i< FILE_LEN /256;i ++)
        GetNextBlockData();    //Get next 256 bytes data to LBA_Buff buffer.
        for(ps_x=0;ps_x<256;ps_x++)
        {
                bit_mask=0x80;
                for(i_mask=0;i_mask<8;i_mask++)
                {
                        SCLK=0;//clk
                        Delay1us();
                        if(LBA_Buff[ps_x] & bit_mask)//data
                                SDO=1;
                        else
                                SDO=0;
                        Delay1us();
                        SCLK=1;//clk
                        Delay1us();
                        bit_mask>>=1;
                }
                Delay1us();
        }
}
CS=1;
 // Addition dummy process
  for(i_mask=0;i_mask<64;i_mask++)
  {
        SCLK=0;//clk
        Delay1us();
        SCLK=1;//clk
         Delay1us();
  }
  SCLK=1;//clk
```